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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,995	03/06/2002	Yasuhiko Matsunaga	220327US2	6814

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,995	MATSUNAGA ET AL.	
	Examiner	Art Unit	
	Connie C. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

2. Claims 1-23 are presented for examination.

Specification

3. The disclosure is objected to because of the following informalities:

On page 14, line 29-30, applicant discussed that "the selected gate transistor SG11 is turned off on the bit line BL1 side". However, on page 14, line 19-21, applicant disclosed that the control line SGD is applied with Vdd, therefore, it is not possible for the SG11 transistor to be in an "off" state.

On page 14, line 34, applicant discussed that a write voltage Vpgm is applied to "a selected second control gate line CG1", however, on page 14, line 15-16, applicant has mentioned it to be "a control gate line CG1" already. Therefore, are these two control gate line CG1 meant to be the same or are they different and how are they different?

Applicants should review and correct the entire specification for misspelling, for example: on page 15 line 6, change "Th " word to –The--. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

The description of "a boosted voltage Vpre higher than Vdd are given to the bit lines BL1" on page 14, line 16-19 of claim 1, 10 and 16 can not be found in figure 3. Figure 3, only show that BL1 receiving a Vdd voltage.

The description of "applying Vdd + alpha to the bit line side select gate line SGD" on page 14, line 19-20 of claim 1, 10 and 16 can not be found in figure 3. Figure 3, only show that SGD receiving a Vdd voltage.

Specification

Title

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1, 10, 16 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In claim 1, 10, 16, lines 19-27, the phrase of "a reference voltage is applied to respective control gates of the two memory transistors each adjacent to said selected memory transistor, to thereby turn off the one of said two adjacent memory transistors on the common source line side, and to turn off or on the one of the two adjacent memory transistors on the bit line side depending upon whether data 1 or 0 is applied to the bit line". Examiner have can not find support in the specification describing the two memory transistor each adjacent to the selected memory transistor. Examiner cannot determine which two transistors especially to figure 3, can be considered the two memory transistors being adjacent to the selected memory transistor.

Claims 2-9, 11-15 and 17-23 are also rejected for the same reason set forth above due to their dependency of the rejected parent claims.

Claim Rejections - 35 USC § 112

7. Claim 1, 10, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 10, and 16 claimed "a first memory transistor, which being non-selected" on line 36-37, and "a third memory transistor, which being non-selected", on line 33-34, without claiming a second memory transistor, which being non-selected. In order to claim a third, applicant must have a first and a second.

There is insufficient antecedent basis for the limitations.

In claim 1,10, 16 recite the limitation "said second memory transistor" on line 31-32.

In claim 1, 10, and 16, examiner in general have a difficulty in understanding how "a selected one of the plurality of memory transistors of the NAND cell" on line 17-18, "the two memory transistors each adjacent to said selected memory transistor" on line 20-23 and "a second one of said memory transistors of said NAND cell from the bit line side" on line 28-29, are layout and operate with respective to each other. Please direct examiner toward which figure and element numbers that best described or represent these transistors so as to guide the examiner to clearly understand the layout and functionality of these transistors in respect to each other.

Conclusion

8. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (703) 306-5731. After January 8, 2004, the new number will be (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached on (703) 308-4910. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

C. Yoha

November 2003

Connie C. Yoha

Patent Examiner

Art Unit 2818